

**Remarks**

Reconsideration of the application is requested. Applicants have canceled the original claims and substituted new claims 40-45, which more particularly claim the patentability of the invention.

Asano, the primary reference cited by the Examiner, discloses a conventional non-volatile semiconductor memory. As such, Asano does not teach or suggest a test structure in which the tunnel openings corresponding to different write paths have different sizes and are tested for sufficiency via a read path coupled to multiple floating gates in the manner claimed.

Chang does not make up for Asano's lack of disclosure in this regard. Chang discloses an EEPROM fabrication technique (Fig. 1) in which it is said that a tunnel area 30 of a minimum size is achievable by using a tunnel opening 28 having dimensions larger than that of the resulting tunnel area and larger than that of the lowest lithographic resolution limit. Col. 5, line 30 to col. 6, line 24. Chang, however, does not disclose structure for testing to determine a minimum size of the tunnel area or of the tunnel opening. A sufficient size is simply assumed, likely determined in advance of fabrication by prior art techniques. Certainly the specifics of the claimed test structure are not shown or suggested.


Moreover, even if the combined references were assumed to disclose the all the elements of the claimed invention, the Examiner has cited no evidence of a specific suggestion, teaching, or motivation to combine these references in the manner claimed.

Applicants believe therefore that the claims are now in condition for allowance, and such action is respectfully requested.

Please call the undersigned if he can be of any further assistance in this case.

Respectfully submitted,

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